AIDA srl was established in 2003 as a spin-off company of the University of Parma by Angelo Farina, Alberto Bellini, Enrico Armelloni, Fabio Bozzoli, Giacomo Frassi, Christian Varani, Gianfranco Cibelli, Erica Pincolini.

Its main business perspective is to design audio equipments and algorithms. Its main skills are in the area of:

- Acoustic measurements and design;
- Electronic design;
- Electromagnetic compatibility.
AIDA Electronic design

The major fields of activity are:

• Design of DSP system;
  • FIR filters.
  • IIR filters.
  • Lattice IIR filters.
  • Warped filters.
  • FFT partitioned convolution.
  • Spectrum Analyzer.
  • 2D Wavelet decomposition.
  • Encoder/Decoder JPEG2000.

• Design of power electronics circuits for audio.
  • DLCF digital audio amplifier.
  • TANDEM hybrid audio amplifier.
  • 3boost power supply.
A number of projects were successfully carried out involving FIR filters. FIR filters were realized for fixed and floating point processors, specifically for SHARC 21065L, SHARC 21161N, BF535, BF533 and BF561. Moreover a dedicated equalization procedure was realized, relying on Aurora plug-ins.

Aurora tools for FIR equalization synthesis

Acoustic measurements after FIR equalization. Solid red line target curve, Solid green line curve with FIR equalization, dashed line original SPL curve. The FIR equalization procedure was presented at AES convention.
IIR filters

A number of projects were successfully carried out involving IIR filters. IIR filters were realized for fixed and floating point processors. Moreover a dedicated four channel DSP processor board (DIGIcar) was realized relying on the TMS320C5402 DSP. Several algorithms were implemented on it, including a 7-band IIR parametric equalizer.

DIGIcar prototype photograph

Acoustic measurements of the DIGIcar board

DIGIcar was presented at IEEE ISCAS 2002.
Lattice IIR filters

Lattice IIR filters for audio applications were developed. Starting from the standard IIR coupled all-pass architecture, a wide range of optimised filters were created for several audio applications:

- Generalized floating point Lattice bandpass and lowpass filter for SHARC processors
- Heavily optimised fixed-point Lattice allpass-based filter for BlackFin processors

As far as the fixed-point version is concerned several structures were benchmarked in order to compare different code realizations:

- 16 bit fixed point Direct Form II
- 16.16 virtual floating point Direct Form II
- 24.8 virtual floating point Direct Form II
- 32 bit fixed point Direct Form II
- 32 bit Lattice coupled allpass

The following chart report the results of the comparison for a single channel input source and for a dual channel input source. It turns out that the computational cost of lattice implementation is the same for single and dual channel input source, since a symmetric architecture is used.

The lattice architecture allows efficient filtering operation and avoids the chronic problems of fixed point implementation.

With fixed point arithmetic the realization of digital filters with cut off frequency close or very far from the sampling frequency is unstable. The use of lattice filter reduce this drawback, thus allowing very low or very high cut-off frequencies. The following figures report the frequency response and the harmonic analysis (with a 1kHz single tone input) of a lattice band pass filter with 1 kHz center frequency, and 48 kHz sampling frequency.
Under the same conditions, the standard Direct Form II IIR filter fixed-point implementation becomes unstable, since of coefficients of the filter are small enough to cause underflows.

References


AIDA staff is interested at improving the sound quality of a car cockpit. To this aim different solutions were investigated, among which one of the most attractive is the development of Warped digital FIR filters (WFIR). This type of filter features a non linear characteristics that fits to the behaviour of human hearing system. Several WFIR were implemented and tested on floating point processors (ADDSP21065L, ADDSP21061, and ADDSP21161N). WFIR filters are also used in Stereo Dipole systems, for cross-talk cancellation filters. The following figures show the results of comparative tests with traditional FIR filters. Objective and subjective tests show that the behaviour at low frequencies is appreciable, where WFIR filters work better than FIR ones even with a reduced (1/5) number of taps.

References


FFT partitioned convolution

Convolution using very long filters is required in order to achieve realistic artificial reverberation, spatial effects or whenever processing of long stream of data is necessary. Unfortunately, DSP (Digital Signal Processors) platforms do not allow real-time implementations of very long digital filters at audio sampling rates, relying on typical time-domain, direct-form algorithms, i.e. FIR or IIR structures. As an example with a clock core of 100 MHz and a sampling frequency of 48 kHz the maximum number of taps for a FIR filter is 2000. Another option is the filtering in the frequency domain using Overlap&Save algorithm, however high latency occurs, and the management of the internal memory of DSP is critical. It turns out that other algorithms are necessary. A real-time partitioned convolution algorithm was realized on both a PC and on a DSP platform (ADDSP21161N). This technique is still based on the Overlap&Save algorithm, but the long impulse responses are partitioned in a reasonable number of equally-sized blocks. Using these algorithms, efficient convolution with long Impulse Responses is obtained, with the advantage of low input/output delay.

Performances reached on DSP platform are listed below.
Partitioned Overlap-and-Save algorithm performance on an Athlon 1000 MHz, 256 kB cache, 266 MHz RAM.

<table>
<thead>
<tr>
<th>IR length</th>
<th>114,688</th>
<th>122,880</th>
<th>126,976</th>
<th>130,048</th>
</tr>
</thead>
<tbody>
<tr>
<td>latency</td>
<td>16384</td>
<td>8192</td>
<td>4096</td>
<td>1024</td>
</tr>
<tr>
<td>exec-time / unpartitioned</td>
<td>0.45</td>
<td>0.71</td>
<td>1.33</td>
<td>5.25</td>
</tr>
<tr>
<td>number of partitions</td>
<td>14</td>
<td>30</td>
<td>62</td>
<td>254</td>
</tr>
</tbody>
</table>

Partitioned Overlap-and-Save algorithm performance on Analog Devices 21161N DSP board

References


AIDAdB is a spectrum analyser system that allows to visualize and to store onto a PDA all the acoustic parameters acquired from a microphone, as recommended into European standards for audio systems.
Specifically AIDAdB acts as a Class 1 audio compliant with European standards EN 61260, EN 60651 and EN 60684, and allows to perform 1/3 or full octave analysis with Fast/Slow/Impulse averages. Moreover it provides the time domain chart and the data logging feature by storing samples into PDA memory.
The core of the system is an ADI BF533 processor on which the signal samples from an external microphone is processed and sent to the PDA using a Bluetooth communication channel. The PDA is simply the Graphical User Interface (GUI) of the spectrum analyzer.

The spectral decomposition of the audio signal is performed by a "analog-behaviour-like" IIR filters bank, as required by the European recommendations.
The original algorithm developed for this purpose, based on AIDA Lattice filters, is patented and allows to dramatically reduce the computational power required for the 1/3 octave decomposition. Specifically the computational cost required for the analysis of one channel, is only the 45% of the computational power available with the DSP clock at 270MHz. Therefore with the BF533 clock at 600 MHz, it is possible to compute up to 4 channel in real time mode.

Another peculiar benefit of the patented algorithm is the possibility of extending the 1/3 octave analysis range down to 0.7 Hz, with a sampling rate of 48kHz. AIDAdB can compute a 22kHz to 0.7Hz spectrum analysis of the signal as required for vibrational applications, with a negligible increase of the required computational power.

In the following figure the performances of the patented algorithm are detailed. The DSP program is running in debug mode controlled by Analog Devices VisualDSP++ Evaluation Tool. Statistical profiling is enabled, and it shows that the DSP processor is idle and stays in a loop (main() procedure) for the 65% of the available time between two data acquisitions.

In the meanwhile CoolEdit Pro generates a test tone (sinusoidal signal at 1 Hz) and the PDA application SonexOne (running in emulation mode on the PC) is displaying the result of the spectral analysis of the test tone.
Computational time profiling for 1/3 octave spectrum analyser (SonexOne application) with a 1Hz sine as input.

References


Wavelet decomposition for image processing

Another topic on digital system tackled by AIDA is video processing. Specifically a wavelet decomposition of images was developed for ADI BF 535, BF 533, BF 561. A complete framework was realized, that includes a dedicated code for Blackfin, a GUI that allows to control program execution, and critical parameters.

![Wavelet decomposition block diagram](image)

As an example the GUI allows to load an image and manage all the parameters involved into a wavelet compression procedure. Data are sent to and from the BlackFin evaluation board that acts as a slave and, once compressed, gives back the image. This GUI is composed by a main interface where a compressed image can be visually compared with original one and with the same image compressed by MATLAB version of the DSP algorithm.

![Matlab GUI](image)

This framework is a valid support in order to develop and test applications much more optimized and oriented toward specific constraints. An attractive option is the possibility to compare results obtained with the reference FIR based wavelet decomposition. Benchmarking is possible also, since it is possible to compute the number of cycle requested by each operation. In the following table some comparisons are reported in tabular version and in graphical format, inside the GUI snapshot. Assembly code and C code were compared to this aim.
Wavelet Decomposition (C implemented) [number of cycles]                JPEG2000 lifting scheme (Assembly implemented) [number of cycles]
Decomposition    169 000 000                                850 000
Composition       120 000 000                                700 000

Comparison on BF533

Matlab GUI and VisualDSP++ interaction: benchmarking options

In summary the Matlab GUI shows its flexibility whenever it is required to test new algorithms and procedures. Thanks to this framework the complete JPEG2000 compression and decompression, was developed for the BlackFin platforms.

References
Digital imaging has had an enormous impact on industrial applications and scientific projects. Consequently image coding and image compression algorithms raised a great commercial interest. The JPEG image coding standard based on DCT (Discrete Cosine Transform) has enjoyed widespread acceptance, and the industry continues to explore its various implementation issues. Because of the many advantages, the top contenders in the upcoming JPEG-2000 standard are all wavelet-based compression algorithms [1], [2], [3], [4].

The AIDA implementation of the JPEG2000 for Blackfin DSP family will be analyzed [5], [6]. The compression is formed by several processes and consequently the algorithm is decomposed into functional block that accomplish simple task and manage a restricted amount of data:
The DWT block is the discrete wavelet transform, that is applied on the individual components of an image, providing reversible (biorthogonal 5-3) or irreversible (Daubechie 9-7) wavelet transformation. This hierarchical approach allows to obtain an extremely modular program with the possibility to modify, substitute or reuse each single function implemented. The overall program is written in C language in order to maintain portability and a good degree of ‘friendliness’ of the overall flux; a JPEG2000 compressor is a complex application for a DSP platform and need to be managed with care in order to maintain the robustness and the flexibility. Moreover thanks to the modularity it is possible to optimize the only the part of code that represent the real bottleneck for what concern the property to be optimized (performances for example). A wide series of compression options as recommended into the standard [7] may be settled, by modifying the relative declaration into the program. The source code was developed for BF 533, and the overall time required to compress the test image (352x288 pixel) is about 276 000 000 cycles. It turns out that the compression takes about 1 second to be completed at 300 MHz. Memory allocation and optimization was handled with particular care. Results are reported in the following pictures for different compression levels.
Original image (BMP, 274Kbytes), compressed to 10Kbytes (top) and heavily compressed to 2Kbytes (bottom).

References


DCLF Amplifier

DCLF double level current feedback digital audio amplifier. A digital audio amplifier combining double level PWM modulation and current feedback was realized with ASK Industries. The project purposes is to realize a high efficiency audio amplifier with a nice distortion level in the whole audio bandwidth.

Experiments show that THD is lower than 1% in the whole audio bandwidth, while efficiency is larger than 87%.

The DCLF architecture was presented in 2003 at AES conventions, [DCLF2003 #6001, #5922].
A hybrid audio amplifier combining a linear and a switching output stage was realized and patented with ASK Industries. The project purpose is to realize a high efficiency audio amplifier with a nice distortion level in the whole audio bandwidth.

Experiments show that the THD is lower than 0.2% in the whole audio bandwidth.

The TANDEM architecture was patented in 2002, and presented at AES 106th convention [TANDEM2004 #6001].
3 boost power supply.

A step-up DC/DC converter for automotive applications was realized and patented with ASK Industries. The project purposes is to realize a high efficiency converter that is fed by a standard battery, and supplies a dual voltage with +30 V, -30 V to an audio amplifier.

Experiments show that the RF (Vac/VDC) is around 0.014% while efficiency is larger than 87%.

The 3boost architecture was patented in 2004.
Environmental sustainability is an emerging topic. Many design activities exist that aim at anticipating and reducing pollution. Geological, acoustic and electromagnetic pollution are among the larger sources of problem. AIDA is involved in analysis of electromagnetic and acoustic pollution. Specifically a 3D CAD of electromagnetic fields for power lines was realized. It is capable of computing both magnetic and electric field at ELF (Extremely Low Frequencies, 0-100 kHz). The numerical core is very flexible and allows several configurations: three-phase and single-phase lines, DC and AC, different shapes (catenary lines, piece wise linear lines).

The GUI is user friendly and allows to insert data and parameters of each power lines, and import from Autocad files is available. Simulation results were compared with experiments in order to validate the effectiveness of the numerical core. Simulation results can be exported in 2D, 3D charts or ASCII format.

Simulation results can be exported in 2D, 3D charts or ASCII text files.
Hereafter sample results are reported.
AIDA staff is available for any customization.